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**APPLICATION FOR LETTERS PATENT**

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**Semiconductor Constructions and Methods of  
Forming Semiconductor Constructions**

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1                    Semiconductor Constructions and Methods of Forming  
2                    Semiconductor Constructions

3                    TECHNICAL FIELD

4                    The invention pertains to methods of forming semiconductor  
5 constructions in which a first semiconductor substrate is bonded to a  
6 second semiconductor substrate. The invention also pertains to  
7 semiconductor constructions comprising a first semiconductor substrate  
8 bonded to a second semiconductor substrate.

9  
10                   BACKGROUND OF THE INVENTION

11                   Technologies referred to as "smart cut" and "wafer-bonding" have  
12 been utilized to bond monocrystalline silicon materials onto  
13 semiconductor substrates. Smart cut technology generally refers to a  
14 process in which a material is implanted into a silicon substrate to a  
15 particular depth and ultimately utilized to crack the substrate, and wafer  
16 bonding technology generally refers to a process in which a first  
17 semiconductive substrate is bonded to a second semiconductor substrate.

18                   In particular applications of smart cut and wafer-bonding  
19 technology, hydrogen ions (which can be, for example,  $H^+$ ,  $H_2^+$ ,  $D^+$ ,  
20  $D_2^+$ ) are implanted into a first monocrystalline silicon substrate to a  
21 desired depth. The first monocrystalline silicon substrate comprises a  
22 silicon dioxide surface, and is bonded to a second monocrystalline  
23 substrate through the silicon dioxide surface. Subsequently, the bonded

1 first substrate is subjected to a thermal treatment which causes cleavage  
2 along the hydrogen ion implant region to split the first substrate at a  
3 pre-defined location. The portion of the first substrate remaining  
4 bonded to the second substrate can then be utilized as a silicon-on-  
5 insulator (SOI) substrate. An exemplary process is described in U.S.  
6 Pat. 5,953,622. The SOI substrate is subsequently annealed at a  
7 temperature of greater than or equal to 900°C to strengthen chemical  
8 coupling within the second substrate.

9 The present invention encompasses new applications for smart cut  
10 and wafer-bonding technology, and new semiconductor structures which  
11 can be created utilizing such applications.

## SUMMARY OF THE INVENTION

In one aspect, the invention includes a method of forming a semiconductor construction. A first substrate is provided which comprises silicon-containing structures separated from one another by an insulative material. The silicon-containing structures define an upper surface. A second semiconductor substrate is provided which comprises a monocrystalline material having a damage region therein. The second semiconductor substrate is bonded to the silicon-containing structures of the first substrate at the upper surface. The monocrystalline material is then cleaved along the damage region.

In another aspect, the invention encompasses another method of forming a semiconductor construction. A first substrate is provided which comprises silicon-containing structures separated from one another by an insulative material. The silicon-containing structures define an upper surface. A second semiconductor substrate is bonded to the silicon-containing structures at the upper surface. The second semiconductor substrate comprises a mono-crystalline material. At least one doped silicon region is formed to extend through the monocrystalline material and to electrically contact at least one of the silicon-containing structures.

In another aspect, the invention encompasses a semiconductor construction comprising a first substrate having silicon-containing structures separated from one another by an insulative material, and a

1 second substrate comprising a monocrystalline material. The silicon-  
2 containing structures of the first substrate define an upper surface, and  
3 the monocrystalline material of the second substrate is bonded over the  
4 silicon-containing structures at the upper surface.

#### 6 BRIEF DESCRIPTION OF THE DRAWINGS

7 Preferred embodiments of the invention are described below with  
8 reference to the following accompanying drawings.

9 Fig. 1 is a diagrammatic, cross-sectional view of a first  
10 semiconductor substrate at a preliminary step of a method of the  
11 present invention.

12 Fig. 2 is a diagrammatic, cross-sectional, fragmentary view of a  
13 second semiconductor substrate at a preliminary step of a method of the  
14 present invention.

15 Fig. 3 is a diagrammatic, cross-sectional, fragmentary view of a  
16 semiconductive material comprising the first substrate of Fig. 1 and the  
17 second substrate of Fig. 2.

18 Fig. 4 is a diagrammatic, cross-sectional, fragmentary view of the  
19 Fig. 3 fragment shown at a processing step subsequent to that of Fig. 3.

20 Fig. 5 is a view of the Fig. 3 fragment shown at a processing step  
21 subsequent to that of Fig. 4.

22 Fig. 6 is a view of the Fig. 3 fragment shown at a processing step  
23 subsequent to that of Fig. 5.

1 Fig. 7 is a view of the Fig. 3 fragment shown at a processing step  
2 subsequent to that of Fig. 6.

3 Fig. 8 is a view of the Fig. 3 fragment shown at a processing step  
4 subsequent to that of Fig. 7.

5 Fig. 9 is a view of the Fig. 3 fragment shown at a processing step  
6 subsequent to that of Fig. 8.

7 Fig. 10 is a view of the Fig. 3 fragment shown at a processing  
8 step subsequent to that of Fig. 9.

9 Fig. 11 is a view of the Fig. 3 fragment shown at a processing  
10 step subsequent to that of Fig. 10.

11 Fig. 12 is a view of the Fig. 3 fragment shown at a processing  
12 step subsequent to that of Fig. 11.

13 Fig. 13 is a view of the Fig. 3 fragment shown at a processing  
14 step subsequent to that of Fig. 12.

15 Fig. 14 is a view of the Fig. 3 fragment shown at a processing  
16 step subsequent to that of Fig. 13.

17 Fig. 15 is a view of the Fig. 3 fragment shown at a processing  
18 step subsequent to that of Fig. 14.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

An exemplary method of the present invention is described with reference to Figs. 1-15. Referring to Fig. 1, a first semiconductor substrate 10 is illustrated in fragmentary view. Substrate 10 comprises a monocrystalline silicon wafer 12 having conductively-doped diffusion regions 14, 16, 18, 20, 22, 37 and 39 therein. Diffusion regions 14, 16, 20, 22, 37 and 39 can comprise, for example, either n-type or p-type conductivity-enhancing dopants. Monocrystalline silicon wafer 12 can comprise a background doping with a p-type dopant. Although wafer 12 is described as comprising monocrystalline silicon, it is to be understood that wafer 12 can comprise other semiconductive materials, including, for example, germanium; or can comprise combinations of semiconductive materials, such as, for example, a combination of silicon and germanium. Wafer 12 can be referred to herein and in the claims that follow as a first base. To aid in interpretation of the claims that follow, the terms "semiconductive substrate" and "semiconductor substrate" are defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive

1 material layers (either alone or in assemblies comprising other  
2 materials). The term "substrate" refers to any supporting structure,  
3 including, but not limited to, the semiconductive substrates described  
4 above.

5 Insulative isolation regions 24 are formed within substrate 12.  
6 Isolation regions 24 can comprise, for example, silicon dioxide, and can  
7 be formed as shallow trench isolation regions.

8 Transistor gates 26 and 28 are formed over substrate 12 and  
9 comprise a gate oxide layer 30, a polysilicon layer 32, a silicide layer 34  
10 and an insulative cap 36. Sidewall spacers 38 are shown formed along  
11 gates 26 and 28. Gate 26, together with diffusion regions 14, 16 and  
12 37, defines a first field effect transistor, and gate 28 together with  
13 diffusion regions 20, 22 and 39 defines a second field effect transistor.  
14 In embodiments in which diffusion regions 14, 16, 20 and 22 are heavier  
15 doped with n-type dopant than p-type dopant, the first and second field  
16 effect transistors comprise NMOS transistors. Alternatively, if diffusion  
17 regions 14, 16, 20 and 22 are heavier doped with p-type dopant than  
18 n-type dopant, the first and second transistors can comprise PMOS  
19 transistors. Regions 37 and 39 can comprise lightly doped diffusion  
20 (Ldd) regions. It is noted that the above-described first and second  
21 field effect transistors are conventional transistor structures, and are  
22 provided as exemplary circuitry comprised by semiconductor substrate 10.  
23 Other circuitry, including other forms of field effect transistors, can be



1 comprised by semiconductor substrate 10 in alternative embodiments of  
2 the present invention.

3 An insulative material 40 is formed over wafer 12, and over  
4 transistor gates 26 and 28. Insulative material 40 can comprise, for  
5 example, silicon dioxide, borophosphosilicate glass (BPSG), or silicon  
6 nitride.

7 Silicon-containing structures 42, 44, 46, 48, 50 and 52 extend at  
8 least partially into insulative material 40, with structures 42, 44, 46, 48  
9 and 52 extending entirely through material 40 to define plugs or  
10 pedestals. It is noted that the structure of Fig. 1 can be considered  
11 as comprising silicon-containing pedestals (defined by, for example,  
12 structures 44 and 46) separated by insulative regions (defined by  
13 insulative material 40), or alternately as comprising insulative pedestals  
14 (defined by insulative material 40) separated by silicon-containing regions  
15 (defined by, for example, structures 44 and 46).

16 The silicon-containing structures 42, 44, 46, 48, 50 and 52 can be  
17 formed by, for example, forming openings in insulative material 40, and  
18 subsequently filling the openings with a silicon-containing material. It  
19 is to be understood that the term silicon-containing structure  
20 encompasses, but is not limited to, structures which consist essentially  
21 of silicon, or consist of silicon. The silicon of structures 42, 44, 46, 48,  
22 50 and 52 can comprise, for example, monocrystalline silicon,  
23 polycrystalline silicon, or amorphous silicon. In particular embodiments,

1 the silicon of structures 42, 44, 46, 48, 50 and 52 can consist essentially  
2 of, for example, conductively-doped monocrystalline silicon, conductively-  
3 doped polycrystalline silicon, or conductively-doped amorphous silicon.

4 Structures 42, 44, 46, 48 and 52 are preferably conductively doped,  
5 as such structures comprise conductive interconnections to diffusion  
6 regions associated with wafer 12. In contrast, structure 50 is shown to  
7 not be connected with other circuit elements, and accordingly can  
8 remain undoped. Structure 50 will be described in the present  
9 disclosure as having no function as an electrical circuit element.  
10 Instead, structure 50 has a sole function of being provided for  
11 utilization in bonding a second semiconductor substrate through  
12 processing which is described below. Structure 50 has a different width  
13 than structures 42, 44, 46, 48 and 52 to emphasize that structure 50 can  
14 be formed by a different pattern than the other structures.

15 Silicon-containing structures 42, 44, 46, 48, 50 and 52 have upper  
16 surfaces 43, 45, 47, 49, 51 and 53, respectively. In the shown  
17 embodiment, such upper surfaces are planarized relative to one another,  
18 and at a common elevation above wafer 12. Surfaces 43, 45, 47, 49,  
19 51 and 53 thus define a common planarized upper surface which can be  
20 utilized in subsequent bonding (described below) to a second  
21 semiconductor substrate. The common upper surface of silicon-  
22 containing structures 42, 44, 46, 48, 50 and 52 can be formed by, for  
23 example, chemical-mechanical polishing. Preferably, such surface is

1 substantially planar to the extent that the roughness of the common  
2 upper surface is defined by less than 5Å root mean square (rms)  
3 variation. More preferably, the roughness is defined by less than 2Å  
4 rms variation.

5 In the shown embodiment, insulative material 40 comprises an  
6 upper surface 41 that is planar and coextensive with the upper surfaces  
7 of silicon-containing structures 42, 44, 46, 48, 50 and 52. The shown  
8 structure can be formed by, for example, chemical-mechanical  
9 planarization of insulative material 40 together with the silicon material  
10 of structures 42, 44, 46, 48, 50 and 52. It is to be understood,  
11 however, that the invention encompasses other embodiments (not shown)  
12 wherein insulative material 40 comprises an upper surface which is  
13 downwardly recessed relative to the upper surfaces of silicon-containing  
14 structures 42, 44, 46, 48, 50 and 52.

15 Fig. 2 shows a second semiconductor substrate 100 comprising a  
16 semiconductive material wafer 102. Substrate 100 can be referred to as  
17 a second base. Semiconductive material wafer 102 can comprise, for  
18 example, monocrystalline silicon, and can be lightly doped with a  
19 background p-type dopant. Substrate 100 comprises a damage  
20 region 104 formed therein. Damage region 104 can be formed by, for  
21 example, implanting hydrogen ions into wafer 102. Wafer 102 has an  
22 upper surface 106 which is preferably substantially planar, with the term  
23

1 "substantially planar" again referring to a surface defined by a  
2 roughness of less than 5Å rms, and more preferably less than 2Å rms.

3 Referring to Fig. 3, second substrate 100 is inverted and bonded  
4 to first substrate 10 to form a structure 200. More specifically,  
5 surface 106 of substrate 102 is bonded to surfaces 43, 45, 47, 49, 51  
6 and 53 of silicon-containing structures 42, 44, 46, 48, 50 and 52.  
7 Surface 106 and surfaces 43, 45, 47, 49, 51 and 53 can be cleaned with,  
8 for example, hydrofluoric acid, immediately prior to the bonding to  
9 remove native oxide from over such surfaces. The bonding of  
10 substrate 100 to substrate 110 preferably comprises a temperature of less  
11 than or equal to about 700°C and can comprise, for example, a  
12 temperature of about 700°C for a time of at least about 15 minutes..  
13 A suitable time can be from about 15 minutes to about two hours.  
14 The bonding can occur under a nitrogen atmosphere at about  
15 atmospheric pressure, or alternatively can occur under a vacuum. A  
16 suitable vacuum is less than or equal to about 500 mTorr, and  
17 preferably less than or equal to about 10 mTorr. In a particular  
18 embodiment, the bonding can comprise a first temperature treatment of  
19 less than about 500°C, and a second temperature treatment of less than  
20 or equal to about 700°C. The treatment occurring at a temperature of  
21 less than about 500°C is utilized as a preliminary bonding prior to  
22 cleaving of substrate 100 (described below with reference to Fig. 4), and  
23 the bonding at 700°C occurs after such cleaving to enhance chemical

1 coupling between substrate 102 and silicon-containing structures 42, 44,  
2 46, 48, 50 and 52.

3 In particular embodiments of the invention, the only temperatures  
4 utilized for bonding are less than or equal to 700°C, and  
5 monocrystalline wafer 12 is not exposed to temperatures  
6 exceeding 700°C after the bonding. An advantage of utilizing  
7 temperatures less than or equal to about 700°C for bonding and  
8 subsequent processing of structure 200 is that such can alleviate  
9 diffusion of dopants within semiconductor substrate 10 relative to  
10 diffusion which would occur at higher temperatures.

11 In embodiments in which diffusion of dopants is not considered  
12 problematic, temperatures above 700°C can be utilized for bonding  
13 substrate 100 to substrate 10. If insulative material 40 comprises silicon  
14 dioxide, such embodiments can comprise temperatures high enough to  
15 bond the silicon dioxide to monocrystalline silicon of base 102, such as,  
16 for example, temperatures of 900°C or greater. In such embodiments,  
17 base 102 will be bonded to upper surfaces 43, 45, 47, 49, 51 and 53 of  
18 silicon-containing structures 42, 44, 46, 48, 50 and 52, and will also be  
19 bonded to upper surface 41 of insulative material 40.

20 If bonding is conducted at temperatures wherein the bonding of  
21 monocrystalline base 102 is only to silicon-containing structures (e.g., 42,  
22 44, 46, 48, 50 and 52), it can be advantageous to add additional silicon-  
23 containing structures to substrate 10. Structure 50 is an exemplary

1 silicon-containing structure which has been added to substrate 10 solely  
2 for the purpose of enhancing bonding. In the shown embodiment,  
3 structure 50 extends only partially through insulative material 40. In  
4 other embodiments, additional silicon-containing structures could be  
5 formed which extend entirely through insulative material 40, and which,  
6 like structure 50, have no function other than bonding of substrate 100  
7 to substrate 10.

8 Referring to Fig. 4, substrate 100 is cleaved along damage  
9 region 104. In embodiments in which damage region 104 corresponds  
10 to a region wherein hydrogen ions were implanted, the cleavage can be  
11 accomplished by thermal processing. Suitable thermal processing can  
12 include, for example, exposure of damage region 104 to a temperature  
13 of greater than or equal to about 500°C.

14 The cleavage leaves a roughened upper surface 202 of  
15 structure 200. Such surface can be planarized by, for example,  
16 chemical-mechanical planarization to form the planar upper surface 204  
17 shown in Fig. 5. In particular embodiments, the thickness of  
18 fragment 102 remaining after cleavage (Fig. 4) is about 0.5 microns, and  
19 the thickness after planarization (Fig. 5) is about 0.3 microns. The  
20 planarization shown in Fig. 5 can be referred to as "smoothing" of the  
21 roughened upper surface 202 of the Fig. 4 structure 200.

22 Figs. 6-15 illustrate formation of insulative and conductive  
23 elements over and on monocrystalline base 102 of structure 200.

1 Referring to Fig. 6, protective layers 205 and 207 (which can comprise,  
2 for example, silicon dioxide and silicon nitride, respectively) are formed,  
3 and a patterned masking layer 206 is formed over the protective layers.  
4 Patterned masking layer 206 can comprise, for example, photoresist, and  
5 can be patterned by photolithographic processing. Patterned masking  
6 layer 206 covers some portions of monocrystalline base 102, while  
7 leaving other portions exposed. Referring to Fig. 7, the exposed  
8 portions of base 102 are removed to leave gaps 210 extending to upper  
9 surfaces of substrate 10. In embodiments in which material 102  
10 comprises monocrystalline silicon, such can be removed by, for example,  
11 an etch utilizing one or more of  $\text{CF}_4$ ,  $\text{O}_2$ , and  $\text{CF}_3\text{Cl}$ .

12 Referring to Fig. 8, gaps 210 (Fig. 7) are filled with insulative  
13 material 212, and masking layer 206 (Fig. 7) and protective layers 205  
14 and 207 are removed. The removal of layers 205, 206 and 207 can be  
15 accomplished by, for example, chemical-mechanical polishing. Insulative  
16 material 212 can comprise, for example, silicon dioxide or silicon nitride.  
17 The processing of Figs. 6-8 can be referred to as a trench/refill process  
18 for forming insulative material within substrate 102. In the shown  
19 embodiment, gaps 210 (Fig. 7) are formed to extend entirely through  
20 base 102, and accordingly, insulative material 212 extends entirely  
21 through base 102. In other embodiments (not shown) at least some of  
22 the gaps can be formed to extend only partially into base 102, and  
23 accordingly at least some of insulative material 212 will extend only

1 partially through base 102. Insulative regions 212 can comprise isolation  
2 regions between devices formed on and within base 102. Although the  
3 shown method of forming isolation regions is a trench/refill method, it  
4 is to be understood that other methods, such as, for example, local  
5 oxidation of silicon, could be utilized for forming isolation regions  
6 within a monocrystalline base 102. The insulative regions are shown  
7 having a planarized upper surface, and such can be accomplished by, for  
8 example, chemical-mechanical polishing. It is noted that the described  
9 trench/refill can comprise forming the insulative material over the  
10 masking layer and within the gaps, and subsequent chemical-mechanical  
11 polishing to leave the insulative material within the gaps while removing  
12 the masking layer and insulative material thereover. Alternatively, the  
13 trench/refill can comprise removing the masking layer prior to forming  
14 the insulative material within the gaps.

15 Referring to Fig. 9, protective layers 217 and 219 (which can  
16 comprise, for example, silicon dioxide and silicon nitride, respectively)  
17 are formed. Subsequently, a patterned masking layer 220 is formed over  
18 the protective layers, over a surface 204 of base 102, and over at least  
19 some of isolation regions 212. Portions of base 102 are covered by  
20 masking layer 220, while other portions are exposed. A pattern is  
21 transferred from masking layer 220 to underlying layers 217 and 219, as  
22 shown.  
23



1 Referring to Fig. 10, the exposed portions of base 102 are  
2 removed to form gaps 222 extending through material 102 and to an  
3 upper surface of substrate 10. Gaps 222 can be formed utilizing  
4 processing similar to that described above with reference to Fig. 7 for  
5 forming gaps 210.

6 Referring to Fig. 11, patterned masking layer 220 (Fig. 10) is  
7 removed and gaps 222 (Fig. 10) are filled with conductive material 224.  
8 Conductive material is typically formed within gaps 222 and over  
9 protective layers 217 and 219 (Fig. 10). Subsequently, the conductive  
10 material is removed from over the protective layers, and the protective  
11 layers are removed from over material 102. Layer 217 and 219 protect  
12 material 102 during removal of conductive material 224, as it can be  
13 difficult to selectively etch a preferred conductive material (doped  
14 silicon) relative to the monocrystalline material 102. A problem that  
15 can occur after forming conductive material 224 in gaps 222 is that  
16 leaky diodes can form at interfaces between material 224 and  
17 monocrystalline material 102. Such problem can be alleviated by lateral  
18 out-diffusion from material 224 into material 102 so that junctions are  
19 formed within material 102 rather than at interfaces of materials 102  
20 and 224. The out-diffusion can be accomplished by, for example, a  
21 thermal treatment, and can laterally out-diffuse dopant to a distance of,  
22 for example, about 100Å into material 102 from the interface of  
23 materials 102 and 224.

1       The conductively doped silicon of material 224 can be in the form  
2 of amorphous silicon, polycrystalline silicon, or monocrystalline silicon.  
3 Conductive material 224 can comprise, either alternatively or in addition  
4 to conductively doped silicon, other conductive materials such as, for  
5 example, metals or metal silicide. If the conductive material 224  
6 comprises doped silicon, such can be either n-type doped silicon or p-  
7 type doped silicon. In particular embodiments it will be heavily n-type  
8 doped silicon (i.e., doped to a concentration greater than  
9  $1 \times 10^{19}$  atoms/cm<sup>3</sup> with an n-type dopant). Although conductive  
10 regions 224 are shown extending entirely through base 102, it is to be  
11 understood that regions 224 can extend either entirely into base 102 as  
12 shown, or only partially into base 102 in other embodiments (not  
13 shown).

14       A patterned masking layer 230 is formed over conductive  
15 material 224, insulative material 212, and some portions of base 102,  
16 while leaving other portions of base 102 exposed. Masking layer 230  
17 can also be formed over channel regions, junction regions, and/or  
18 shallow trench isolation regions. A conductivity enhancing dopant 232  
19 is implanted into the exposed portions of base 102 to form threshold  
20 voltage ( $V_t$ ) implant regions 233 within base 102. The  $V_t$  implant  
21 regions can extend entirely through base 102, or only partially into  
22 base 102. The  $V_t$  implant regions can be formed with a blanket  
23 implant into an entirety of an upper surface of semiconductive material

102, and/or can be implanted through patterned photoresist for special adjustments. In exemplary applications, openings for  $V_t$  implants could extend over at least one channel and one or more of junctions and isolation regions.

Referring to Fig. 12, masking layer 230 (Fig. 11) is removed and transistor gates 240 and 242 are formed over the  $V_t$  implant regions 233. Transistor gates 240 and 242 comprise a gate oxide layer 244, a polysilicon layer 246, a metal silicide layer 248 and an insulative cap 250. Transistor gates 240 and 242 are conventional transistor gate structures, and provided as exemplary embodiments of transistor gates which can be formed. It is to be understood that other types of transistor gates, as well as other circuit devices, can be formed over base 102.

Referring to Fig. 13, a patterned masking layer is formed over some of base 102, while leaving transistors gate 240 and 242, and regions proximate transistor gates 240 and 242, exposed. Insulative material sidewall spacers 272 are shown formed along sidewalls of transistor gate 242, and not along sidewalls of gate 240. Sidewall spacers 272 can be formed by conventional methods, including, by depositing and subsequently anisotropically etching an insulative material. the spacers can be selectively formed to be only along sidewalls of gate 242, and not along sidewalls of gate 240, by, for example, initially forming spacers along sidewalls of both of gates 240 and 242, and

1 subsequently protecting the spacers along gate 242 while etching the  
2 spacers from along gate 240. Sidewall spacers 272 can comprise, for  
3 example, silicon dioxide or silicon nitride. In typical processing, a  
4 protective mask would be formed over transistor gate 240 while sidewall  
5 spacers 272 are formed alongside transistor gate 242. Alternatively,  
6 spacers could be formed alongside sidewalls of gate 240, as well as  
7 alongside the sidewalls of gate 242.

8 Source/drain regions 274 and 275 are implanted proximate gates  
9 240 and 242, and Ldd regions 277 are implanted between source/drain  
10 regions 274 and gate 242. Ldd regions 277 can be implanted prior to  
11 formation of spacers 272, or with an angled implant after formation of  
12 spacers 272. Gate 242 and source/drain regions 274 define a field  
13 effect transistor, while gate 240 and source/drain regions 275 define  
14 another field effect transistor. In the shown embodiment, source/drain  
15 regions 274 are implanted only partially into base 102. It is to be  
16 understood, however, that the invention encompasses other embodiments  
17 wherein source/drain regions are implanted deep enough into base 102  
18 to extend entirely through the base.

19 Source/drain regions 275 are, in addition to being source/drain  
20 regions, conductive interconnections between circuitry above base 102  
21 and circuitry below base 102. Specifically, source/drain regions 275  
22 interconnect with regions 224, which in turn interconnect to circuitry  
23 beneath base 102. The regions 224 interconnect with source/drain

1 regions 275 can be considered extensions of the source/drain regions.  
2 Source drain regions 275 allow some misalignment of patterning to form  
3 transistor gate 240, as the regions 275 will extend between gate 240 and  
4 regions 224 regardless of whether gate 240 is precisely centered between  
5 adjacent regions 224 or not.

6 Referring to Fig. 14, masking layer 270 (Fig. 13) is removed, and  
7 an insulative material 280 is formed over substrate 100 and transistor  
8 gates 240 and 242. Insulative material 280 can comprise, for example,  
9 BPSG.

10 Referring to Fig. 15, openings are etched into insulative  
11 material 280 and conductive structures 282, 284 and 286 are formed  
12 within the openings. Conductive structures 282, 284 and 286 can  
13 comprise, for example, one or more of conductively-doped amorphous  
14 silicon, polycrystalline silicon, or monocrystalline silicon. Structures 282,  
15 284 and 286 can thus comprise silicon-containing structures. In  
16 subsequent processing (not shown) another semiconductor substrate can  
17 be bonded to silicon-containing structures 282, 284 and 286 and  
18 processing analogous to that of Figs. 6-15 repeated to form circuitry on  
19 the next semiconductor substrate. Accordingly, a stack of semiconductor  
20 substrates and circuitry can be formed.

21 In other embodiments, structures 282, 284 and 286 can comprise  
22 other conductive materials besides silicon, such as, for example, metals  
23 and/or metal silicides.

1 In particular processing, at least one of the transistors comprising  
2 gates 26 and 28 between semiconductive material bases 12 and 102 is  
3 of a different type than at least one of the transistors comprising gates  
4 that are on semiconductive material base 102. For instance, at least  
5 one of the transistors comprising gates 26 and 28 can be a PMOS  
6 transistor, and at least one of the transistors comprising gates 240  
7 and 242 can be an NMOS transistor. In other embodiments, one type  
8 of transistor will be formed over base 102 which is not formed between  
9 bases 102 and 12. For instance, only n-type transistors can be formed  
10 between bases 102 and 12, and both n-type and p-type transistors can  
11 be formed over base 102. In still other embodiments, one type of  
12 transistor will be formed over between bases 12 and 102 which is not  
13 formed over base 102. For instance, only n-type transistors can be  
14 formed over base 102, and both n-type and p-type transistors can be  
15 formed between bases 12 and 102.

16 Processing of the present invention can be utilized with either or  
17 both of logic and memory device constructions. In particular  
18 embodiments the processing can be utilized to form DRAM  
19 constructions having increased device density and increased data  
20 retention relative to conventional DRAM constructions.

21 In compliance with the statute, the invention has been described  
22 in language more or less specific as to structural and methodical  
23 features. It is to be understood, however, that the invention is not

1 limited to the specific features shown and described, since the means  
2 herein disclosed comprise preferred forms of putting the invention into  
3 effect. The invention is, therefore, claimed in any of its forms or  
4 modifications within the proper scope of the appended claims  
5 appropriately interpreted in accordance with the doctrine of equivalents.  
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